Supply Voltage Biasing: A Knob for Scaling FinFETs

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**ABSTRACT**

As transistors continue to scale, short channel effects (SCEs) in planar metal-oxide semiconductor field-effect transistors (MOSFETs) become more prevalent. These SCEs serve to reduce the performance and success rate in MOSFETs. Fin-shaped field effect transistors (FinFETs) are a new MOSFET technology popular for their resistance to SCEs and ability to scale down power consumption and area in integrated circuits (ICs). However, due to a fin which protrudes from the Si body and acts as the channel, FinFETs are resistant to body effects. Therefore, as MOSFETs are scaled down and FinFETs become more prevalent, an alternate knob to body biasing is required. In this paper, we present a new gate configuration designed and implemented to enable supply voltage biasing. With simulations using the FreePDK, we saw a 15% maximum decrease in delay with forward supply biasing and a 38% decrease in both static and active power under reverse bias compared to the design under no bias.

# INTRODUCTION

As transistors continue to scale, short channel effects (SCEs) in traditional planar metal-oxide semiconductor field-effect transistors (MOSFETs) become more prevalent. These SCEs serve to decrease MOSFET performance and reliability. There are many emerging designs which mitigate these performance-hindering effects, including nanowires [3], [10], high-k dielectrics [1], and tunnel FETs [4], [5]. Perhaps the most promising of these designs is the Fin-shaped field-effect transistor (FinFET). A FinFET is a three-dimensional structure with a gate that wraps around a fin that protrudes from the bulk silicon. FinFETs show considerable resistance to SCEs compared to planar MOSFETs, as well as improved drive strength per unit silicon [7]. Because the silicon fin is often fabricated in a manner that completely isolates it from the bulk, they are immune to body effects [6]. Although these body effects can cause problems in the operation of FETs (e.g. performance degradation), they can also be exploited as a knob to modulate the threshold voltage of a transistor. Therefore, we seek a new knob as MOSFETs continue to scale and FinFETs become more prevalent.

In this paper, we present a novel design for supply biasing gates, which can be implemented in both planar MOSFETs and FinFETs. We present the results for our preliminary simulations of inverter, NAND, and NOR gates in ring oscillator configurations. We then present and discuss the design of an 8-bit ripple carry adder implementing our supply bias design, and compare simulation results from that to results of a similar ripple carry adder which does not implement our design. When discussing the 8-bit adder, we first consider a non-biased adder that consists of half the number of transistors used in our supply bias gate design. Then, we evaluate a non-biased adder with transistors twice as large as those in our supply bias design, in order to conduct a comparison between two configurations that have similar surface area requirements. Our goal is to prove that the supply biased design can effectively decrease delay in forward bias and decrease static power in reverse bias.

# RELATED WORK

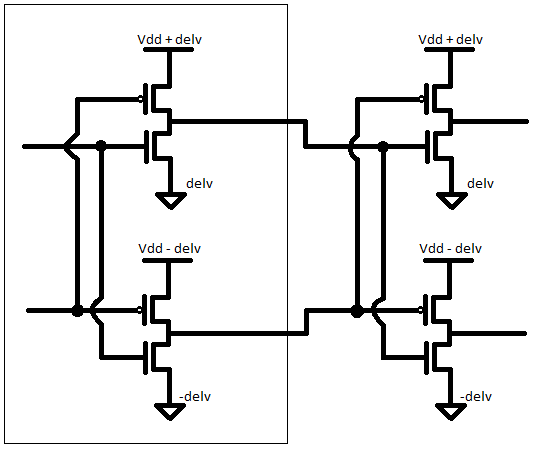
Adaptive supply voltage is an active area of research. As far as we are aware, no papers have been written on our proposed supply bias gate design or on supply voltage biasing with respect to scaling FinFETs. The most closely related approach to our work is in adaptive body biasaing. In [8], Tschanz et al. use bidirectional adaptive body bias to compensate for local and global die variations. There are also a number of evaluations of supply voltage bias and body bias for typical planar MOSFETs. In [2], Chen et al. present a detailed comparison between adaptive body bias and adaptive source voltage for managing delay and leakage due to process variation. Similarly, in [9], Tschanz et al. evaluate the effectiveness of adaptive supply voltage and body bias for influencing variations in high performance low power microprocessors.

# SIMULATION

All simulations are conducted using the Cadence design environment and the 45 nm FreePDK.

## Supply Biased Inverter Gate

**Supply Biased Inverter Gate Configuration**



**Figure 1. The outlined circuitry is what we consider one gate. Notice that there are two outputs; one that is shifted up by a bias voltage (*delv*), and one that is shifted down. The output from the up-shifted gate is connected to the next gate’s NMOS transistors while the output from the down-shifted gate is tied to the next gate’s PMOS transistors.**

Our general design for the supply biased gate consists of two similar gates. The supplies to one of the gates are shifted up by some bias voltage *delv*, while the supplies to the other gate are shifted down by *delv*. Therefore, a single gate of our design requires two inputs and produces two outputs—one high and one low. Figure 1 illustrates this design for a supply biased inverter gate. The output from the up-shifted gate is tied to both NMOS gate inputs to “overdrive” them during a high output. The output from the down-shifted gate is tied to both PMOS transistor gate inputs for the same reason. It may be clear that when biased with a positive voltage this design has the potential to increase the drive strength, and therefore speed of the FETs. Note, however, that a negative bias voltage will drive the gate-to-source voltage of the receiving gate (the gate not within the rectangle in Figure 1) below zero in half of the “off” transistors, which leads to a decrease in static power. We will discuss these effects in the next section.

## Ring Oscillator

We instrumented our supply biased inverter gate in an 11-gate ring oscillator configuration. The metrics of interest were the frequency of the ring oscillator in active mode and the static power in inactive mode as compared to the bias voltage. The nominal voltage for the ring oscillator was set at 1.1 V, and the bias voltage was swept from -100 mV to 100 mV in 10 mV intervals. The frequency response is plotted in Figure 2.

**Figure 2. Normalized frequency response versus bias voltage of 11-gate supply biased ring oscillator. We see a maximum increase in frequency of ~15% at 100 mV.**

Under the maximum bias, we were able to achieve an increase in frequency of 15%. It may be observed that the trend in Figure 2 could allow us to increase the frequency further if we were to increase the bias voltage past 100 mV. We will give an explanation for our voltage bias bounds in Section 3.3.

In order to evaluate how the static power changes with the applied bias voltage, we fixed a node of our ring oscillator by connecting it to a voltage supply; this ensured a node was held constant and prevented the circuit from oscillating. Figure 3 (a) illustrates how the static power scales with the bias voltage across the full range of bias, while Figure 3 (b) shows the static power in reverse bias.

The static power in the supply biased ring oscillator increases exponentially under forward (positive *delv*) bias. This is due to the linearly increasing gate-to-source voltage on “off” transistors, which causes leakage current of those transistors to increase exponentially. In reverse bias, the static power appears to reach an optimum point at a bias of around -45 mV. We discuss this phenomenon further in the next section.

**(a)**

**(b)**

**Figure 3. (a) Static power of the ring oscillator as our bias voltage is varied once again from -100 mV to 100 mV; and (b) static power of the ring oscillator with reverse biasing. (b) is a “zoomed” version of (a). In (b), we observe that with reverse bias static power reaches an optimum point at ~-45 mV that is not visible in (a) due to the rapid exponential growth that occurs starting at a bias voltage of ~-40 mV.**

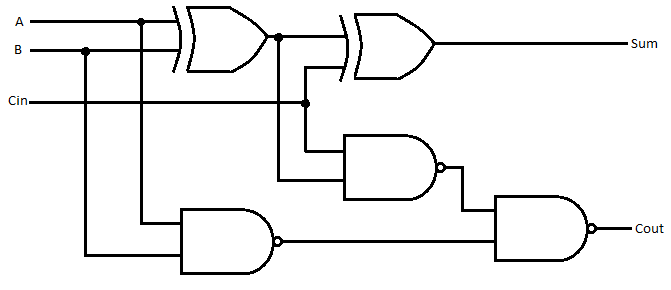
We next implemented our design in supply biased NAND and NOR gates. Like the inverter, the NAND and NOR gates had twice as many transistors as their standard CMOS counterpart, and two outputs: one high and one low. The NAND and NOR gates were also set up in ring oscillator configurations, both with 11 gates. We conducted the same analysis as with the inverter ring oscillator and found that these gates react very similarly to supply biasing. We opted not to display these results because we feel they do not contribute anything beyond our findings for the 11-inverter ring oscillator.

## Ripple Carry Adder

Using the inverter, NAND, and NOR gates mentioned in the preceding sections, we designed a CMOS full adder implementing the supply bias configuration. Figure 4 illustrates the full adder design we used to develop a supply biased ripple carry adder.

We developed an 8-bit ripple carry adder (RCA) using the Cadence design environment. The inputs to the RCA were buffered by two of the aforementioned supply biased inverter gates, and the outputs of the RCA drove supply biased inverter gates with transistors four times wider, simulating a fan-out of 4.

**Full Adder Design**



**Figure 4. The two XOR gates designed to evaluate the sum bit were implemented using two NOR gates, one NAND and one inverter gate. In the supply biased design there are twice as many inputs and outputs as those shown here; this schematic is presented to show the full adder design we implemented.**

We set the nominal voltage to 1 V and swept the bias voltage from -100 mV to 100 mV. The metrics of interest for this simulation were the delay of the RCA after a change in the inputs and the static power when the inputs were held constant. We also analyzed the power during a switch, which we comment on later in this section. Figure 5 shows the delay response of the final sum bit to evaluate correctly versus the bias voltage.

**Figure 5. The normalized delay for the final sum bit of the supply biased 8-bit ripple carry adder compared with bias voltage.**

Similar to the ring oscillator, we were able to realize a 15% decrease in delay at the maximum bias voltage. The trend as we increase the bias alludes to the possibility of decreasing delay even further, just as the frequency in the ring oscillator appeared to have the potential to be increased further. If we examine the supply bias design in Figure 1, we can see that a bias voltage of 100 mV leads to a gate-to-source voltage of 200 mV for one of the “off” transistors in the second gate (for a low output from the first gate in Figure 1, the NMOS in the up-shifted part of the second gate has a Vgs of 200 mV, and for a high output from the first gate, the PMOS of the down-shifted part of the second gate has a Vgs of 200 mV). The threshold voltages of the FETs in this technology are about 400 mV. Given this metric, it can be easily deduced that we would not want our bias voltage to exceed 200 mV to prevent any of the “off” transistors from turning on. However, due to process variation, this threshold voltage may dip down well below 400 mV in practice. As such, we decided not to sweep the bias voltage any higher than 100 mV.

**(a)**

**(b)**

**Figure 6. (a) Static power of supply biased RCA in reverse bias; and (b) Switching power of RCA across full swing of bias voltage.**

Figure 6 (a) and (b) illustrate the static power in reverse bias and switching power of the RCA across the full swing of the bias voltage, respectively. The static power was measured before the inputs switched, while the switching power is a measure of the average power consumed during a change in inputs and outputs.

Like the results for the ring oscillator, there appears to be an optimal reverse bias voltage which maximally reduces the static power of the RCA, beyond which it increases. At this optimal point, we simulated a 38% reduction in static power in our RCA compared to the same implementation under zero bias. We were able to realize a 37% decrease in switching power at full reverse bias.

# DISCUSSION

We compare the results from section 3.3 to a control set of values in order to evaluate their significance beyond their ability to modulate delay and power in this design. Our control set consisted of a standard CMOS 8-bit RCA constructed with transistors of equal width to those from the supply biased design, such that our control set occupies only half the area of our design. We found that under no bias the supply bias configuration exhibited a delay that was about 4% smaller than that of the standard RCA. This means that under high forward bias (100 mV) we could achieve a 19% decrease in delay with our supply biased implementation compared to a standard 8-bit RCA with identically sized transistors. We found that the standard RCA exhibited static and switching powers that were half that of the supply biased RCA under no bias. In our simulations we were only able to reduce the static power by 38% in reverse bias; we would need to reduce it by 50% to reach the static power consumed by the standard RCA. To understand the significance of these measurements, it is important to more closely analyze the plots of static power. We see that in deep (>50 mV) reverse bias, the static power actually begins to rise above the minimum. This phenomenon is caused by gate induced drain leakage (GIDL). GIDL is the tunneling of carriers through the ultra-thin gate oxide when the gate and drain are at significantly different voltages. Recall that the PDK used in these simulations is for planar MOSFETs, and not FinFETs. Therefore, we cannot draw any quantitative conclusions from the static power analysis as it applies to FinFETs (our original motivation). We can conclude, however, that static power can be reduced under reverse bias.

# CONCLUSION

As scaling MOSFETs becomes more complex, FinFETs have emerged as a new technology popular for a variety of traits, two of which are their ability to scale down power consumption and area in ICs. In this paper, we designed and tested supply biased gate configurations to evaluate the effectiveness of supply voltage biasing as an alternative to body biasing. We implemented our design first in a simple 2-inverter gate setup, and then used the freePDK to simulate a supply biased 11-inverter ring oscillator. We, lastly, evaluated the performance of a supply voltage biased 8-bit ripple carry adder and compared its behavior to a variety of non-biased configurations with comparable area. Our results show we can achieve a maximum decrease in delay of 15% under forward bias, as well as a 38% decrease in both static and active power under reverse bias compared to the design under no bias. All simulations utilized the 45 nm FreePDK in the Cadence design environment, which to the best of our knowledge does not yet have a FinFET instance available. Therefore, all designs were implemented using planar MOSFETs. The aim of this project was to determine the effectiveness of varying supply voltage as a new knob. Though we cannot draw any quantitative conclusions with respect to FinFETs, we can conclude that supply voltage biasing is an effective knob for which one could construct a power-delay Pareto curve.

# ACKNOWLEDGMENTS

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